8098/8398/8798
COMMERCIAL/EXPRESS HMOS MICROCONTROLLER

- **8798: an 8098 with 8 Kbytes of On-Chip EPROM**
- **8398: an 8098 with 8 Kbytes of On-Chip ROM**

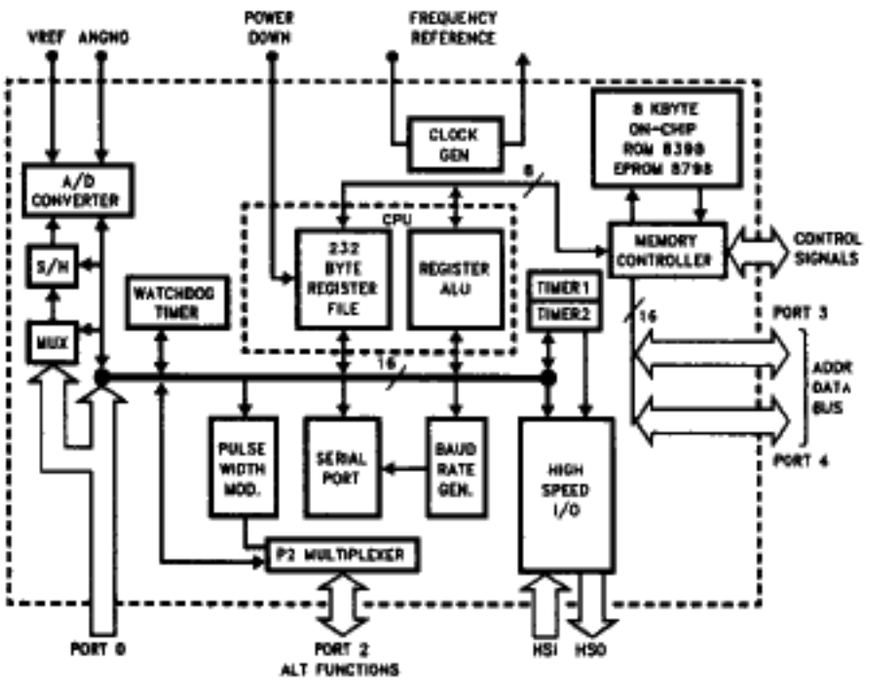
- **232 Byte Register File**
- **Register-to-Register Architecture**
- **10-Bit A/D Converter with S/H**
- **Two 8-Bit and Two 4-Bit I/O Ports**
- **20 Interrupt Sources**
- **Pulse-Width Modulated Output**
- **ROM/EPROM Lock**
- **High Speed I/O Subsystem**
- **Extended Temperature Available**
- **Full Duplex Serial Port**
- **Dedicated Baud Rate Generator**
- **6.25 μs 16 x 16 Multiply**
- **6.25 μs 32/16 Divide**
- **16-Bit Watchdog Timer**
- **Four 16-Bit Software Timers**
- **Two 16-Bit Counter/Timers**
- **Run-Time Programmable EPROM**
- **Extended Burn-In Available**

The MCS®-96 family of 16-bit microcontrollers consists of many members, all of which are designed for high-speed control functions. The 8X98 members were designed specifically for those applications that require the speed of a 16-bit microcontroller but are limited by board space and cost requirements to an 8-bit external bus. The 8X96 members are produced using Intel's HMOS-III process.

The CPU supports bit, byte, and word operations. Thirty-two bit double-words are supported for a subset of the instruction set. With a 12 MHz input frequency the 8098 can do a 16-bit addition in 1.0 μs and a 16 x 16-bit multiply or 32/16 divide in 6.25 μs. Instruction execution times average 1 to 2 μs in typical applications.

Four high-speed trigger inputs are provided to record the times at which external events occur. Six high-speed pulse generator outputs are provided to trigger external events at preset times. The high-speed output unit can simultaneously perform software timer functions. Up to four 16-bit software timers can be in operation at once.

The on-chip A/D converter includes a Sample and Hold, and converts up to 4 multiplexed analog input channels to 10-bit digital values. With a 12 MHz crystal, each conversion takes 22 μs.



270532-1

Figure 1. 8X98 Block Diagram

Also provided on-chip are a serial port, a Watchdog Timer and a pulse-width modulated output signal.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. Unless otherwise noted, the specifications are the same for both options.

With the extended burn-in option, the burn-in is dynamic for a minimum time of 160 hours at 125°C with V_{CC} = 5.5V ±0.5V, following the guidelines in MIL-STD-883, Method 1015.

See the Packaging information for extended temperature and extended burn-in designators.

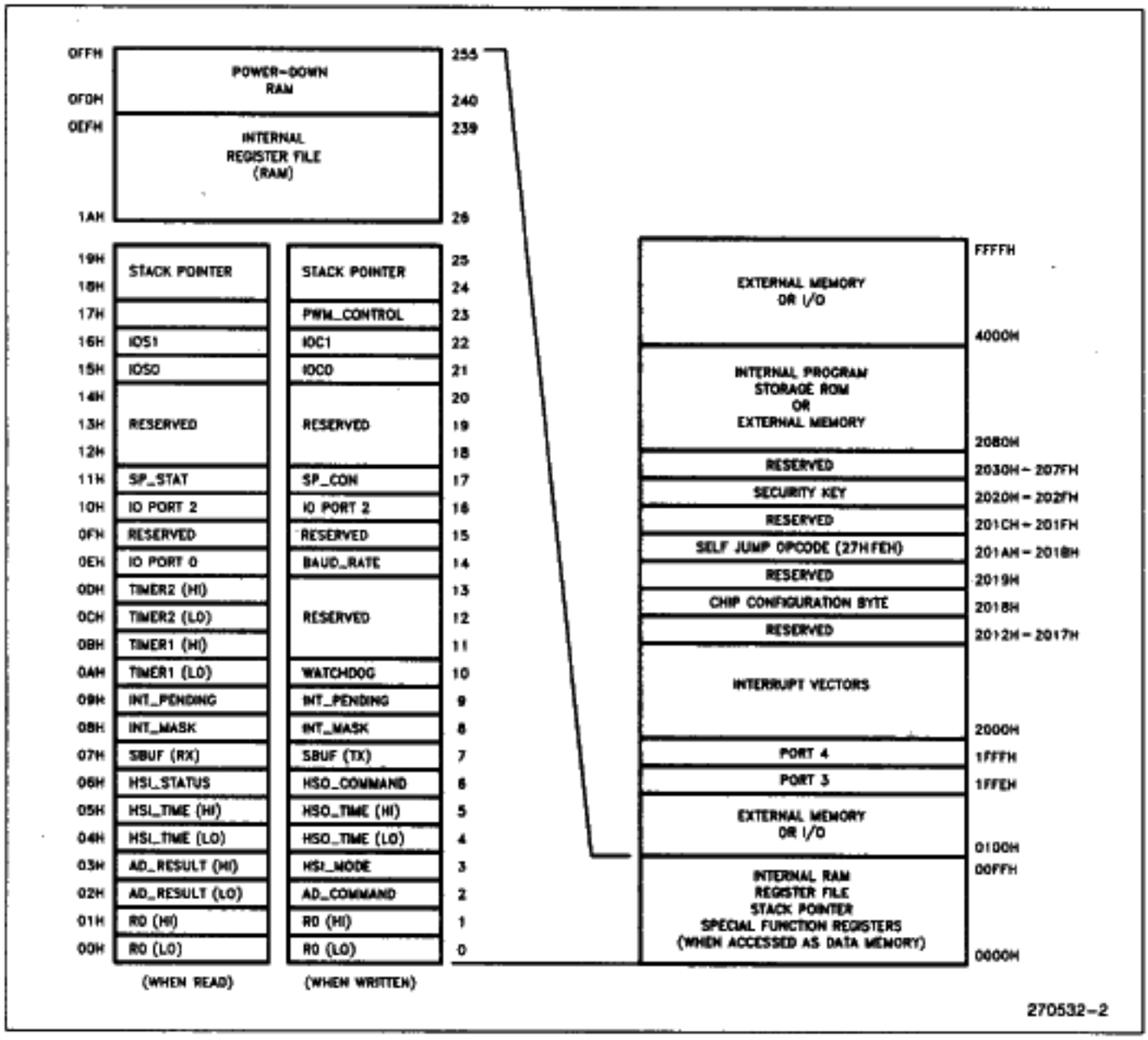


Figure 2. 8X98 Memory Map

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PACKAGING

The 8098 is available in a 48-pin package with and without on-chip ROM or EPROM. The MCS-96 numbering system for the 8X98 devices is shown in Figure 4. Figure 6 shows the pinout for the 48-pin package. The 48-pin version is offered in a Dual-In-Line package.

Factory Masked ROM	CPU	User Programmable	
		EPROM	OTP
48-Pin	48-Pin	48-Pin	48-Pin
8398	8098	8798	8798

Figure 3. MCS®-96 Packaging—8098

Package Designators:
C = Ceramic DIP
P = Plastic DIP

Prefix Designators:
T = Extended Temperature
L = Extended Temperature with 160 Hours Burn-In

Package Type	θ_{ja}	θ_{jc}
48L Plastic DIP	38°C/W	19°C/W
48L Ceramic DIP	26°C/W	6.5°C/W

Figure 4. 8X98 Thermal Characteristics

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

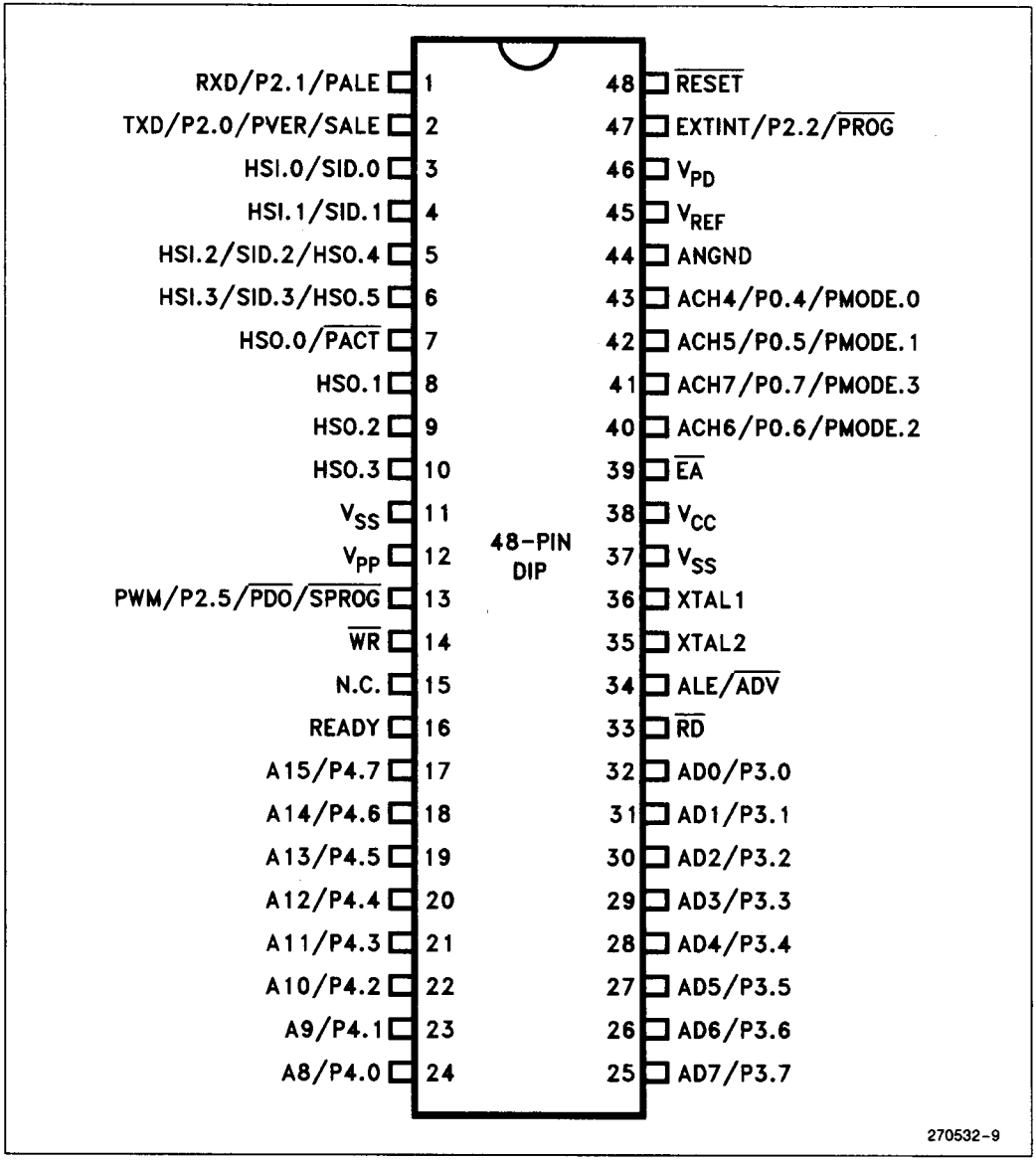


Figure 5. 48-Pin Package

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are two V_{SS} pins, both of which must be connected.
V_{PD}	RAM standby supply voltage (5V). This voltage must be present during normal operation. In a Power Down condition (i.e. V_{CC} drops to zero), if $\overline{RESET}$ is activated before V_{CC} drops below spec and V_{PD} continues to be held within spec., the top 16 bytes in the Register File will retain their contents.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage for the EPROM devices. It should be 12.75V when programming and will float to 5V otherwise. The pin should not be above V_{CC} for ROM or CPU devices. This pin must float in the application circuit on EPROM devices.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
$\overline{RESET}$	Reset input to the chip. Input low for a minimum 10XTAL1 cycles to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time RESET sequence.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM. $\overline{EA}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory. $\overline{EA}$ equal to +12.75V causes the device to enter the Programming Mode.
ALE/$\overline{ADV}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{ADV}$ is activated only during external memory accesses.
$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads.
$\overline{WR}$	Write output to external memory. $\overline{WR}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition of CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available in the CCR.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	4-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 2	4-bit multi-functional port. Its pins are shared with other functions in the 8098.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Ports 3 and 4 are also used as a command, address and data path by EPROM devices in the Programming Mode.
PMODE	Determines the EPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming Mode indicates that programming is in progress. A high signal indicates programming is complete.
PVAL	A low signal in Auto Programming Mode indicates that the device programmed correctly.
SALE	A falling edge in Auto Programming Mode indicates that Ports 3 and 4 contain valid programming address/command information (output from master).
$\overline{\text{SPROG}}$	A falling edge in Auto Programming Mode indicates that Ports 3 and 4 contain valid programming data (output from master).
SID	Assigns a pin of Ports 3 and 4 to each slave to pass programming verification.
PALE	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that Ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that Ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
PVAL	A high signal in Slave Programming Mode indicates the device programmed correctly.
$\overline{\text{PDO}}$	A low signal in Slave Programming Mode indicates that the PROG pulse was applied for longer than allowed.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias −55°C to +125°C

Storage Temperature .....−60°C to +150°C

Voltage from $\overline{EA}$ or V_{PP} to V_{SS} or ANGND .....−0.3V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND .....−0.3V to +7.0V(1)

Average Output Current from Any Pin .....10 mA

Power Dissipation(2) 1.5W

NOTES:
1. This includes V_{PP} on ROM and CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics specified in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias **Commercial** Temp.	0	+70	C
T_A	Ambient Temperature Under Bias **Extended** Temp.	−40	+85	C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	6.0	12	MHz
V_{PD}	Power-Down Supply Voltage	4.50	5.50	V

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current **Commercial** Temp.		240	mA	All Outputs Disconnected.
I_{CC}	V_{CC} Supply Current **Extended** Temp.		270	mA	
I_{CC}	V_{CC} Supply Current ($T_A \geq 70°C$)		185	mA	
I_{PD}	V_{PD} Supply Current		1	mA	Normal operation and Power-Down.
I_{REF}	V_{REF} Supply Current **Commercial** Temp.		8	mA	
I_{REF}	V_{REF} Supply Current **Extended** Temp.		10	mA	
V_{IL}	Input Low Voltage	−0.3	+0.8	V	

DC CHARACTERISTICS (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IH}	Input High Voltage (Except $\overline{RESET}$, NMI, XTAL1)	2.0	$V_{CC}+0.5$	V	
V_{IH1}	Input High Voltage, $\overline{RESET}$ Rising	2.4	$V_{CC}+0.5$	V	
V_{IH2}	Input High Voltage, $\overline{RESET}$ Falling Hysteresis	2.1	$V_{CC}+0.5$	V	
V_{IH3}	Input High Voltage, NMI, XTAL1	2.2	$V_{CC}+0.5$	V	
I_{LI}	Input Leakage Current to each pin of HSI, P3, P4, and to P2.1.		±10	μA	V_{in} = 0 to V_{CC}
I_{LI1}	DC Input Leakage Current to each pin of P0		+3	μA	V_{in} = 0 to V_{CC}
I_{IH}	Input High Current to $\overline{EA}$		100	μA	V_{IH} = 2.4V
I_{IL}	Input Low Current to each pin of P1 and to P2.6, P2.7 **Commercial** Temp.		−125	μA	V_{IL} = 0.45V
I_{IL}	Input Low Current to each pin of P1 and to P2.6, P2.7 **Extended** Temp.		−150	μA	
I_{IL1}	Input Low Current to $\overline{RESET}$	−0.25	−2	mA	V_{IL} = 0.45V
I_{IL2}	Input Low Current P2.2		−50	μA	V_{IL} = 0.45V
V_{OL}	Output Low Voltage on P3, P4 when used as ports		0.45	V	I_{OL} = 0.8 mA (Note 1)
V_{OL1}	Output Low Voltage on P3, P4 when used as ports		0.75	V	I_{OL} = 2.0 mA (Notes 1, 2, 3)
V_{OL2}	Output Low Voltage on Standard Output pins, $\overline{RESET}$ and Bus/Control Pins		0.45	V	I_{OL} = 2.0 mA (Notes 1, 2, 3)
V_{OH1}	Output High Voltage on Standard Output pins and Bus/Control pins	2.4		V	I_{OH} = −200 μA (Note 1)
I_{OH3}	Output High Current on $\overline{RESET}$	−50		μA	V_{OH} = 2.4V
C_S	Pin Capacitance (Any Pin to V_{SS})		10	pF	F_{TEST} = 1.0 MHz

NOTES:
1. Standard Output Pins include TXD, RXD (Mode 0 only), PWM, and HSO pins. Bus/Control pins include ALE, $\overline{RD}$, $\overline{WR}$, AD0–AD7 and A8–A15.
2. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V.
   I_{OL} on Ports 3 and 4 when used as ports: 4.0 mA
   I_{OL} on standard output pins and $\overline{RESET}$: 8.0 mA
   I_{OL} on Bus/Control pins: 2.0 mA
3. During normal (non-transient) operation the following limits apply:
   Total I_{OL} on P2.0, $\overline{RESET}$ and all HSO pins must not exceed 15 mA.
   Total I_{OL} on Port 3 must not exceed 10 mA.
   Total I_{OL} on P2.5 and Port 4 must not exceed 20 mA.

7

AC CHARACTERISTICS Test Conditions: Load Capacitance on Output Pins = 80 pF

TIMING REQUIREMENTS (The system must meet these specifications to work with the 8X98.)

Symbol	Parameter	Min	Max	Units
T_{LLYV}	End of ALE/$\overline{ADV}$ to READY Valid		$2\,T_{OSC} - 70$	ns
T_{LLYH}	End of ALE/$\overline{ADV}$ to READY High	$2\,T_{OSC} + 40$	$4\,T_{OSC} - 80$	ns
T_{YLYH}	Non-Ready Time		1000	ns
T_{AVDV}(1)	Address Valid to Input Data Valid		$5\,T_{OSC} - 120$(2)	ns
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$3\,T_{OSC} - 100$(2)	ns
T_{RHDX}	Data Hold after $\overline{RD}$ Inactive	0		ns
T_{RHDZ}	$\overline{RD}$ Inactive to Input Data Float	0	$T_{OSC} - 25$	ns

NOTE:
1. The term "Address Valid" applies to A0–A15.
2. If wait states are used, add 3 Tosc * N where N = number of states.

TIMING RESPONSES (8X98 devices meet these specs.)

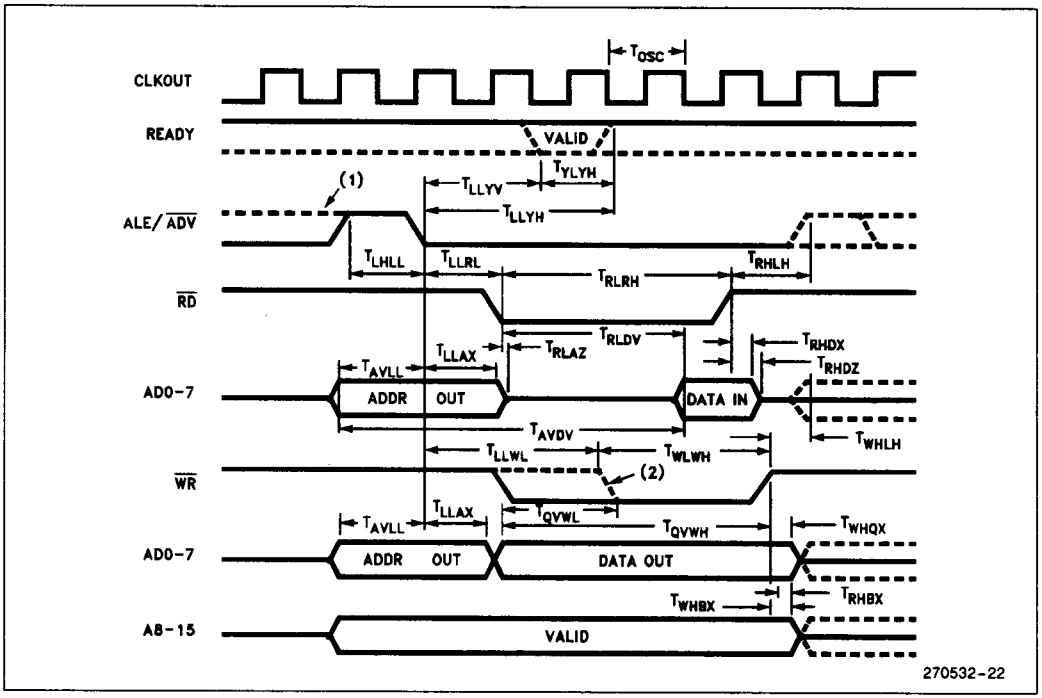
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Oscillator Frequency	6.0	12.0	MHz
T_{OSC}	Oscillator Period	83	166	ns
T_{LHLL}	ALE/$\overline{ADV}$ High Time	$T_{OSC} - 30$	$T_{OSC} + 35$(3)	ns
T_{AVLL}(4)	Address Setup to End of ALE/$\overline{ADV}$	$T_{OSC} - 50$		ns
T_{RLAZ}(5)	$\overline{RD}$ or $\overline{WR}$ Low to Address Float **Commercial** Temp.	Typ. = 0	10	ns
T_{RLAZ}(5)	$\overline{RD}$ or $\overline{WR}$ Low to Address Float **Extended** Temp.		25	ns
T_{LLRL}	End of ALE/$\overline{ADV}$ to $\overline{RD}$ Active	$T_{OSC} - 40$		ns
T_{LLAX}(5)	Address Hold after End of ALE/$\overline{ADV}$	$T_{OSC} - 40$		ns
T_{WLWH}(6)	$\overline{WR}$ Pulse Width	$3\,T_{OSC} - 35$(2)		ns
T_{WLWH}(7)	$\overline{WR}$ Pulse Width	$2\,T_{OSC} - 35$(2)	$2\,T_{OSC} + 40$	ns
T_{QVWH}	Output Data Valid to End of $\overline{WR}$	$3\,T_{OSC} - 60$(2)		ns
T_{WHQX}	Output Data Hold after $\overline{WR}$	$T_{OSC} - 50$		ns
T_{WHLH}	End of $\overline{WR}$ to ALE/$\overline{ADV}$ High	$T_{OSC} - 75$		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	$3\,T_{OSC} - 30$(2)		ns

TIMING RESPONSES (8X98 devices meet these specs.) (Continued)

Symbol	Parameter	Min	Max	Units
T_{RHLH}	End of $\overline{RD}$ to ALE/$\overline{ADV}$ High	T_{OSC} − 45		ns
T_{RHBX}	$\overline{RD}$ High to A8–A15 Inactive	T_{OSC} − 25	T_{OSC} + 30	ns
T_{WHBX}	$\overline{WR}$ High to A8–A15 Inactive	T_{OSC} − 50	T_{OSC} + 100	ns
T_{LLWL}(6)	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	T_{OSC} − 40		ns
T_{LLWL}(7)	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	2 T_{OSC} − 30	2 T_{OSC} + 55	ns
T_{QVWL}(6)	Output Data Valid to $\overline{WR}$ Low	T_{OSC} − 60		ns
T_{QVWL}(7)	Output Data Valid to $\overline{WR}$ Low	T_{OSC} − 30		ns

NOTES:
2. If more than one wait state is desired, add 3 Tosc for each additional wait state.
3. Max spec applies only to ALE. Min spec applies to both ALE and $\overline{ADV}$.
4. The term "Address Valid" applies to AD0–AD7, A8–A15.
5. The term "Address" in this definition applies to AD0–AD7.
6. Write Strobe Mode is not selected.
7. Write Strobe Mode is selected.

WAVEFORM—SYSTEM BUS TIMINGS



NOTES:
1. When $\overline{ADV}$ selected.
2. When Write Strobe Mode selected

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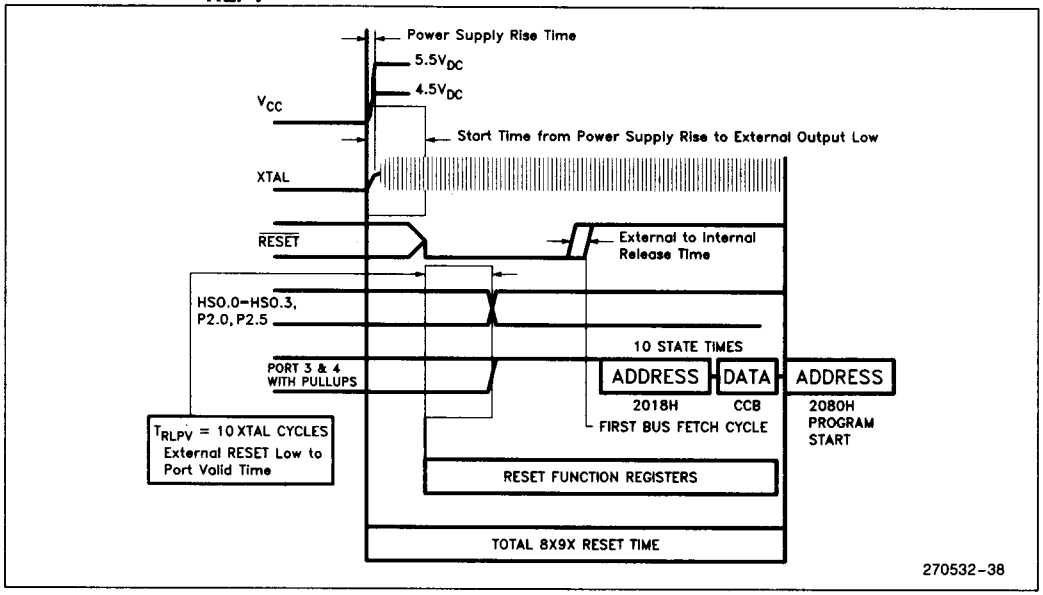
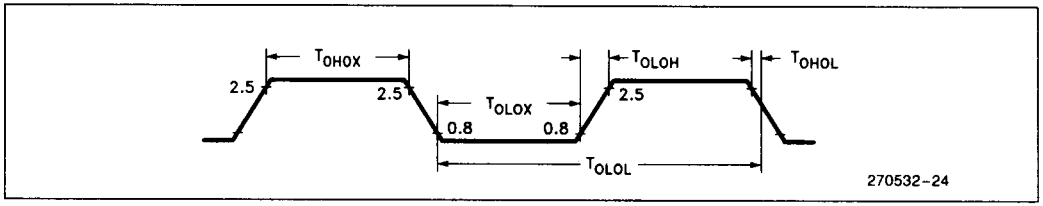
WAVEFORM—T_{RLPV}



EXTERNAL CLOCK DRIVE

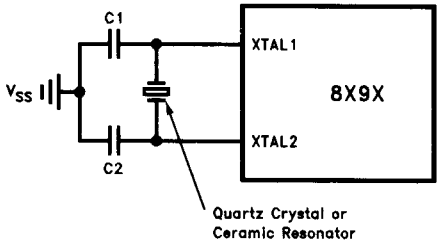
Symbol	Parameter	Min	Max	Units
$1/T_{OLOL}$	Oscillator Frequency	6	12	MHz
T_{OHOX}	High Time	25		ns
T_{OLOX}	Low Time	30		ns
T_{OLOH}	Rise Time		15	ns
T_{OHOL}	Fall Time		15	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

EXTERNAL CRYSTAL CONNECTIONS



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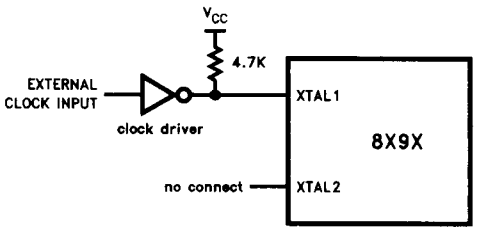
NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 30 pF, C2 = 30 pF. When using ceramic resonators, consult manufacturer for recommended capacitor values.

EXTERNAL CLOCK CONNECTIONS



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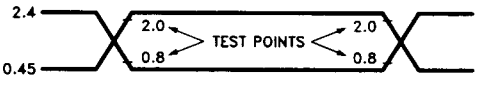
AC TESTING INPUT, OUTPUT WAVEFORMS



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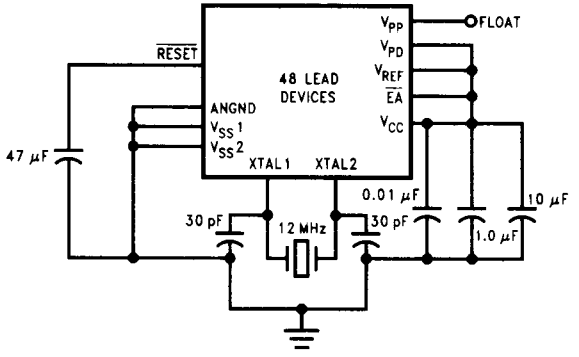
AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS

270532-26

For Timing Purposes a Port Pin is no Longer Floating when a 200 mV change from Load Voltage Occurs, and Begins to Float when a 200 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} \geq \pm 8$ mA.

MINIMUM HARDWARE CONFIGURATION CIRCUIT



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7

AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

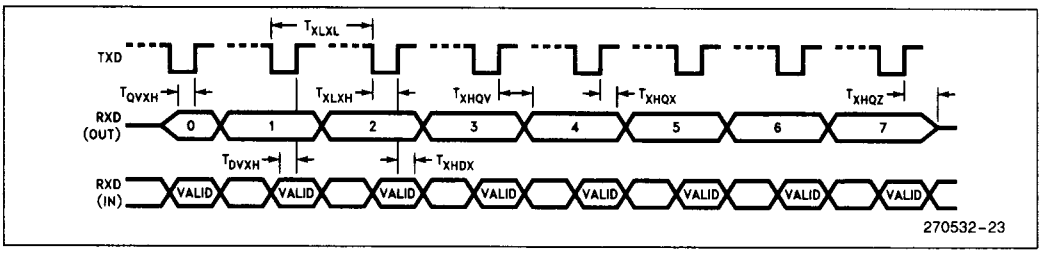
SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Load Capacitance = 80 pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	2 T_{OSC} − 70		ns
T_{XHQV}	Next Output Data Valid After Clock Rising Edge		2 T_{OSC} +50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		5 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



A/D CONVERTER SPECIFICATIONS

The absolute conversion accuracy is dependent on the accuracy and stability of V_{REF}.

See the MCS-96 A/D Converter Quick Reference for definition of A/D Converter Terms.

Parameter	Typical*(1)	Minimum	Maximum	Units**	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±4	LSBs	
Full Scale Error	−0.5 ±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±4	LSBs	
Differential Non-Linearity		> −1	+2	LSBs	
Channel-to-Channel Matching		0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	1, 3
Feedthrough	−60			dB	1
V_{CC} Power Supply Rejection	−60			dB	1
Input Series Resistance		1K	5K	Ω	4
DC Input Leakage		0	3.0	μA	
Sample Delay		$3\,T_{OSC} - 50$	$3\,T_{OSC} + 50$	ns	2
Sample Time		$12\,T_{OSC} - 50$	$12\,T_{OSC} + 50$	ns	
Sampling Capacitor	2			pF	

NOTES:

* These values are expected for most parts at 25°C.

** An "LSB", as used here, is defined in the MCS-96 A/D Converter Quick Reference and has a value of approximately 5 mV.

1. DC to 100 KHz.
2. For starting the A/D with an HSO Command.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

7

EPROM SPECIFICATIONS

EPROM PROGRAMMING OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}, V_{PD}, V_{REF}(1)	Supply Voltages during Programming	4.5	5.5	V
V_{EA}	Programming Mode Supply Voltage	9.0	13.0	V(2)
V_{PP}	EPROM Programming Supply Voltage	12.50	13.0	V(2)
V_{SS}, ANGND(3)	Digital and Analog Ground	0	0	V
$F_{OSC}1$	Oscillator Frequency during Auto and Slave Programming	6.0	6.0	MHz
$F_{OSC}2$	Oscillator Frequency during Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC}, V_{PD} and V_{REF} should nominally be at the same voltage during programming.
2. V_{EA} and V_{PP} must never exceed the maximum voltage for any amount of time or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same voltage (0V) during programming.

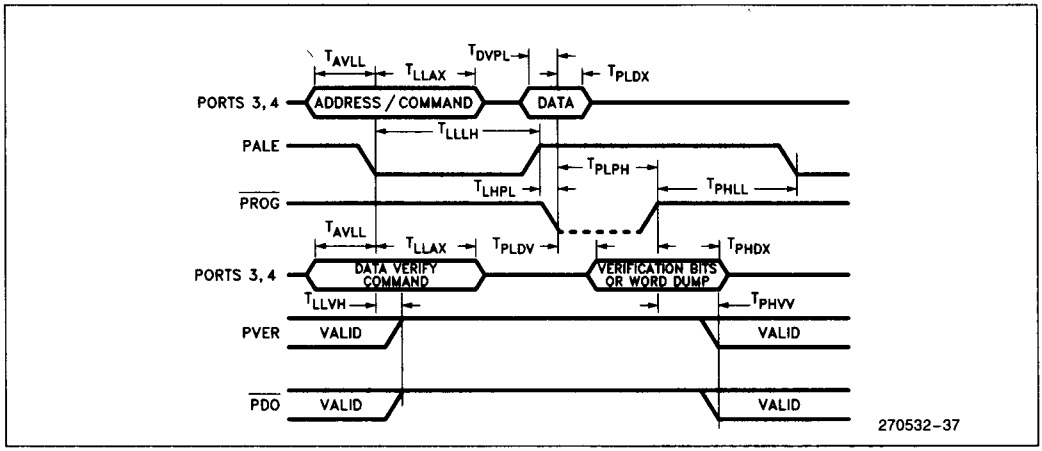
AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
T_{AVLL}	ADDRESS/COMMAND Valid to PALE Low	0		T_{OSC}
T_{LLAX}	ADDRESS/COMMAND Hold After PALE Low	80		T_{OSC}
T_{DVPL}	Output Data Setup Before $\overline{PROG}$ Low	0		T_{OSC}
T_{PLDX}	Data Hold After $\overline{PROG}$ Falling	80		T_{OSC}
T_{LLLH}	PALE Pulse Width	180		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width	250 T_{OSC}	100 µs + 144 T_{OSC}	
T_{LHPL}	PALE High to $\overline{PROG}$ Low	250		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next PALE Low	600		T_{OSC}
T_{PHDX}	Data Hold After $\overline{PROG}$ High	30		T_{OSC}
T_{PHVV}	$\overline{PROG}$ High to PVER/$\overline{PDO}$ Valid	500		T_{OSC}
T_{LLVH}	PALE Low to PVER/$\overline{PDO}$ High	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to VERIFICATION/DUMP Data Valid	100		T_{OSC}
T_{SHLL}	RESET High to First PALE Low (not shown)	2000		T_{OSC}

DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Supply Current (Whenever Programming)		100	mA

WAVEFORM—EPROM PROGRAMMING



DIFFERENCES BETWEEN THE 8X9XBH AND 8X98

1. CCB.1 must be set to a logical 0 on the 8X98.
2. The following 8X9XBH pins and corresponding functions are not available on the 8X98:

   BUSWIDTH

   CLKOUT

   INST

   NMI

   Port 0.0–0.3 (ACH0–3)

   Port 1.0–1.7

   Port 2.6

   Port 2.7

   P2.3 (T2CLK)

   P2.4 (T2RST).

8X98 ERRATA

Devices covered by this data sheet (see Revision History) have the following errata.

1. INDEXED, 3 OPERAND MULTIPLY

The displacement portion of an indexed, three operand (byte or word) multiply may not be in the range of 200H thru 17FFH inclusive. If you must use these displacements, execute an indexed, two operand multiply and a move if necessary.

2. HSI FIFO OPERATION

The High Speed Input (HSI) has three deviations from the specifications. Note that "events" are defined as one or more pin transitions. "Entries" are defined as the recording of one or more events.

A. The resolution is nine states instead of eight states. Events occurring on the same pin more frequently than once every nine states may be lost.

B. A mismatch between the nine state HSI resolution and the eight state hardware timer causes one time-tag value to be skipped every nine timer counts. Events may receive a time-tag one count later than expected.

C. If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register, leaving the FIFO empty again. The next event that occurs will be the first event loaded into the empty FIFO. If the first two events into an **empty** FIFO (not counting the Holding Register) occur coincident with each other, both are recorded as one entry with one time-tag. If the second event occurs within nine states after the first, the events will be entered separately with time-tags at least one count apart. If the second event enters the FIFO coincident with the "skipped" time-tag situation (see B above) the time-tags will be at least two counts apart.

3. RESERVED LOCATION 2019H

The 1990 Architectural Overview recommended that address 2019H be filled with hex value 0FFH. The recommendation is now 20H.

4. RESERVED LOCATION 201CH

Reading reserved location 201CH, either internally or externally, will return "201C" as data.

5. SERIAL PORT SECTION

Serial Port Flags—Reading SP_STAT may not clear the TI or RI flag if that flag was set within two state times prior to the read. In addition, the parity error bit (RPE/RB8) may not be correct if it is read within two state times after RI is set. Use the following code to replace ORB sp_image, SP_STAT.

```
SP_READ:  LDB  TEMP, SP_STAT
          ORB  SP_IMAGE, TEMP
          JBS  TEMP, 5, SP_READ; if
          TI is set then read again
          JBS  TEMP, 6, SP_READ; if
          RI is set then read again
          ANDB SP_IMAGE,#7FH; clear
          false RB8/RPE
          ORB  SP_IMAGE, TEMP; load
          correct RB8/RPE
```

DATA SHEET REVISION HISTORY

This data sheet (270532-008) is valid for devices with an "E" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The difference between -007 and -008 is the I_{OL}/I_{OH} for the float waveform testing changed from ±15 mA to ±8 mA.

The following differences exist between (-007) data sheet and the (-006).

1. The Express (extended temperature and burn-in options) were added to this data sheet. The 8X98 Express data sheet (270914-002) is now obsolete.
2. Changes were made to the format of the data sheet and the SFR descriptions were removed. No specification changes were made.
3. Added Reserved Location 201CH errata.

The following differences exist between the -006 data sheet and the -005 data sheet.

1. The -005 data sheet was valid for devices marked with a "D" at the end of the top side tracking number.
2. The following errata were removed: RESET and the Quasi-Bidirectional Ports, Software RESET Timing, and Using T2CLK as the source for Timer2.
3. The HSI FIFO Operation errata definition was changed to match a change in the HSI FIFO operation.

The following differences exist between the -005 data sheet and the -004 data sheet.

1. Most of the functional description has been removed. This information is in the MCS-96 Architectural Overview.
2. Information on programming the Chip Configuration Register has been added.
3. T_{XHQX} changed from Min = 2 T_{OSC} − 50 ns to Min = 2 T_{OSC} − 70 ns.
4. T_{QLOX} changed from Min = 25 ns to Min = 30 ns.
5. Added AC timings specifications to clarify Write Strobe Mode specifications.
6. The differences between the 8X9XBH and the 8X98 have been added.
7. An errata has been added changing the recommendation for address 2019H from 0FFH to 20H.

Differences between the -004 and -003 data sheets.

1. All EPROM programming mode information has been moved to the Hardware Design Information Chapter.
2. CCB RESET FETCH and JBS/JBC on Port 0 anamolies have been corrected on the current steppings of the 8X98.
3. New information regarding T2CLK and new information about RESET of the Quasi Ports have been added to the Errata section.
4. The Extended Reset errata has been eliminated on the silicon and in the data sheet.
5. HSI Mode register is undefined until the user code initializes this register.
6. Minimum DNL us now > −1 LSB.
7. HSI FIFO overflow description added.

Differences between the -002 and -003 data sheets.

1. All 8798 EPROM information has been added as a complete section after the Analog Section.
2. The chip configuration byte values now indicate the use of WRITE STROBE with 8-bit systems. Write Strobe design text was added to the explanation.
3. The interrupt information now includes a worst case timing diagram.
4. The EPROM 8798 was added as necessary throughout the text.
5. NMI pin information was deleted.
6. Reset Register Status was added and the state of the HSO pins after RESET.
7. A diagram of the Interrupt Pending Register is now included.

8. A diagram of the PSW Register was added.
9. V_{IL1} was deleted. This was a RESET pin characteristic that has been improved to match the other characteristics.
10. The Differential Non-Linearity specification in the A/D converter specifications was corrected to read +2 LSBs.
11. Power On Reset — New information on Extended Reset Time was added to the Errata Section.